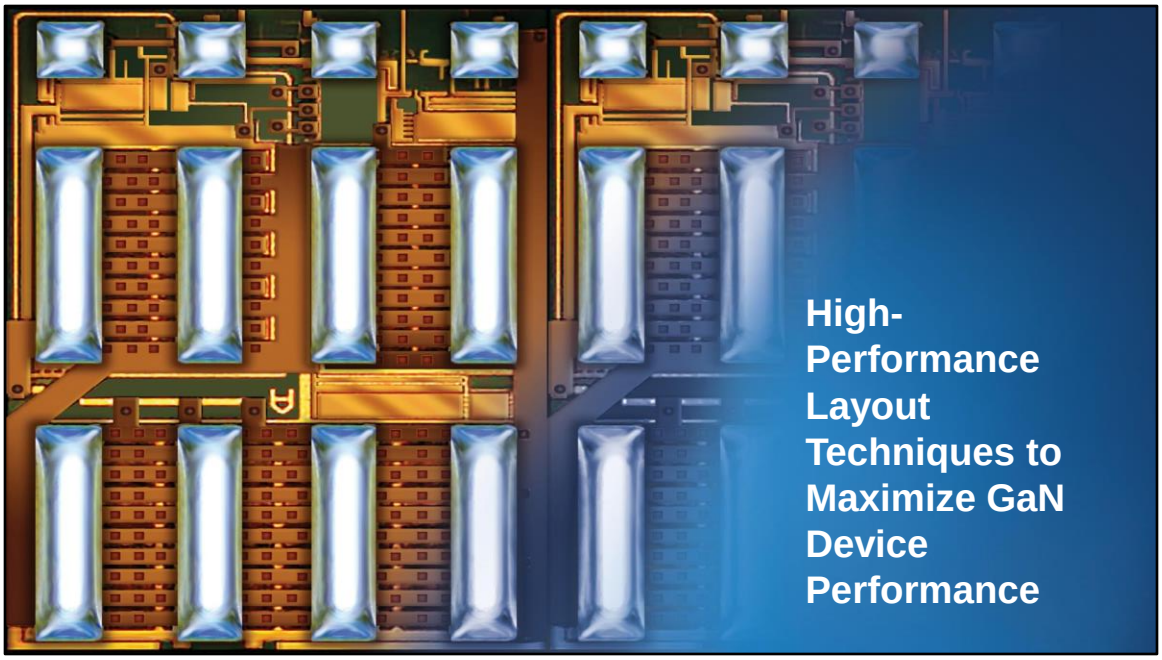


Welcome to the first installment of our How2GaN summer series. In this webinar, we will discuss layout techniques that will maximize the performance of your GaN FET converter

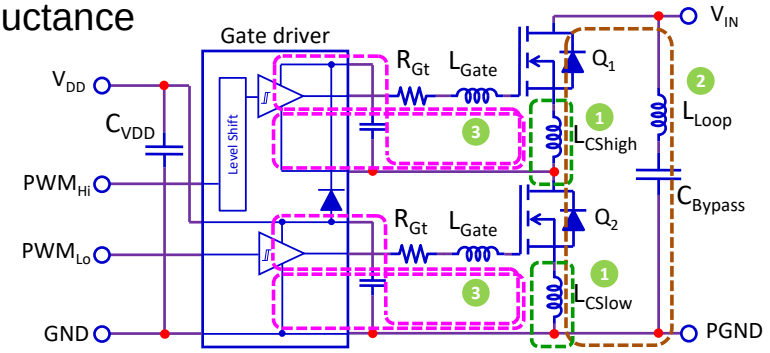
High Performance Layout Techniques

- Parasitic Inductances and their Impact on Converter Performance
- Layout Design Comparisons
- Designing a Low Inductance Layout
- Alternative Layout Configurations
- Gate Circuit Layout
- Working with Single IC Dual Gate Drivers
- Considerations to Add a Source Shunt

Layout is a key factor in determining the performance of a converter. First, we'll look at the various parasitic inductances present in a layout and their impact on the converter's performance. [1] With this knowledge, we can compare various layout designs and learn which ones are best and present [2] additional details on how to design such a layout. Using that information we'll be in a position to look [3] at alternative configurations and operating situations for which each are best suited. [4] After the we'll look at the gate driver circuit layout and how to deal with dual driver IC's. [5] Finally, we'll end this section by looking at how to use the same techniques to include a Source shunt.

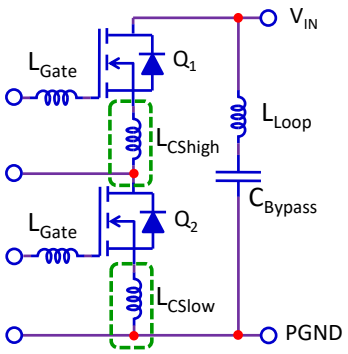
Parasitic Inductance Considerations

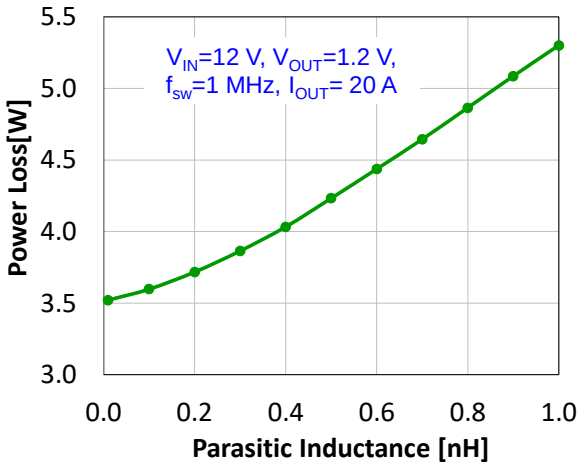
1. Common source inductance
2. Power loop inductance
3. Gate loop inductance
   - Turn-on
   - Turn-off



The main parasitic inductances in a layout are; [1] Common-source inductance form by the sharing of inductance between the gate circuit and the power circuit. [2] Next is the power loop inductance that encompasses both FETs and the decoupling capacitors. [3] Lastly, there is the gate loop inductance which are actually two circuits, [4] one for turn on and [5] the other for turn off.

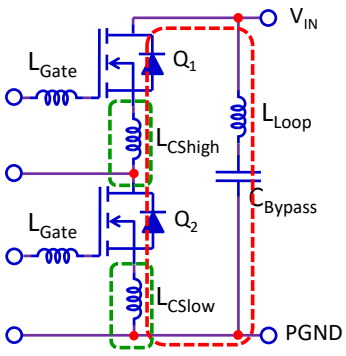
Impact of Common Source Inductance

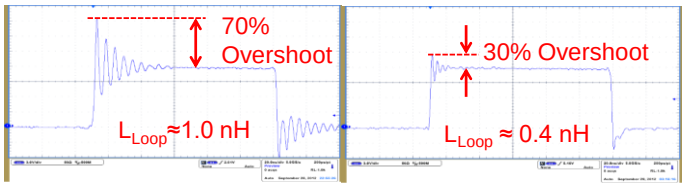


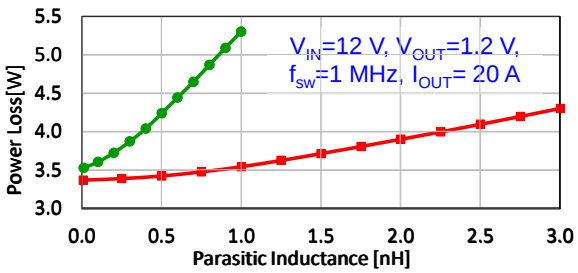


Here we show the impact of common-source inductance on losses generated in the converter. The graph shows the common-source inductance on the x-axis and power loss on the y-axis. As the common source inductance increases, so do the losses generated in the converter. This is due to the slowing down effect on the gate as a result of the opposing voltage generated by the common source current during the transition event. The faster the transition, the higher the opposing effect becomes. The best method to over-come common-source inductance is to eliminate it. We'll show you how layout can achieve this.

Impact of Power Loop Inductance





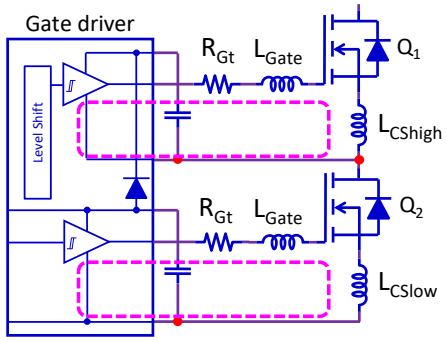


Power Conversion Technology Leader epc-co.com 5

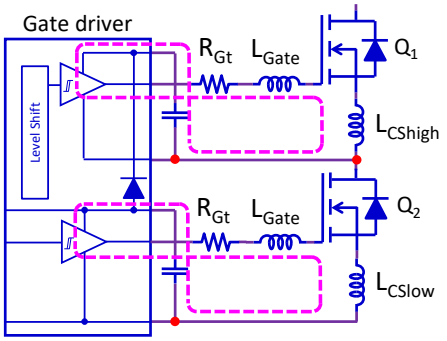
Next is the effect of the power loop inductance on losses generated in the converter. The graph shows the power-loop inductance on the x-axis and power loss on the y-axis. As the power-loop inductance increases, so do the losses generated in the converter. This is due in part to losses resulting from the exchange of energy between the output capacitance of the FETs and the loop inductance. [1] The effect of power-loop inductance can also be observed from the switch-node waveform. The higher power-loop inductance the higher the ringing amplitude. The best method to over-come power-loop inductance is to minimize it. We'll show you how layout can achieve this. [2] Circling back to common-source induced losses we now plot on the same graph thus emphasizing its higher detrimental effect and hence why we always prioritize correcting common-source inductance over power loop inductance.

Impact of Gate Loop Inductance

- Two loops to consider: Turn-on & Turn-off
- L_{Gate} requires R_{Gt} to damp ringing overshoot
  - slows transition

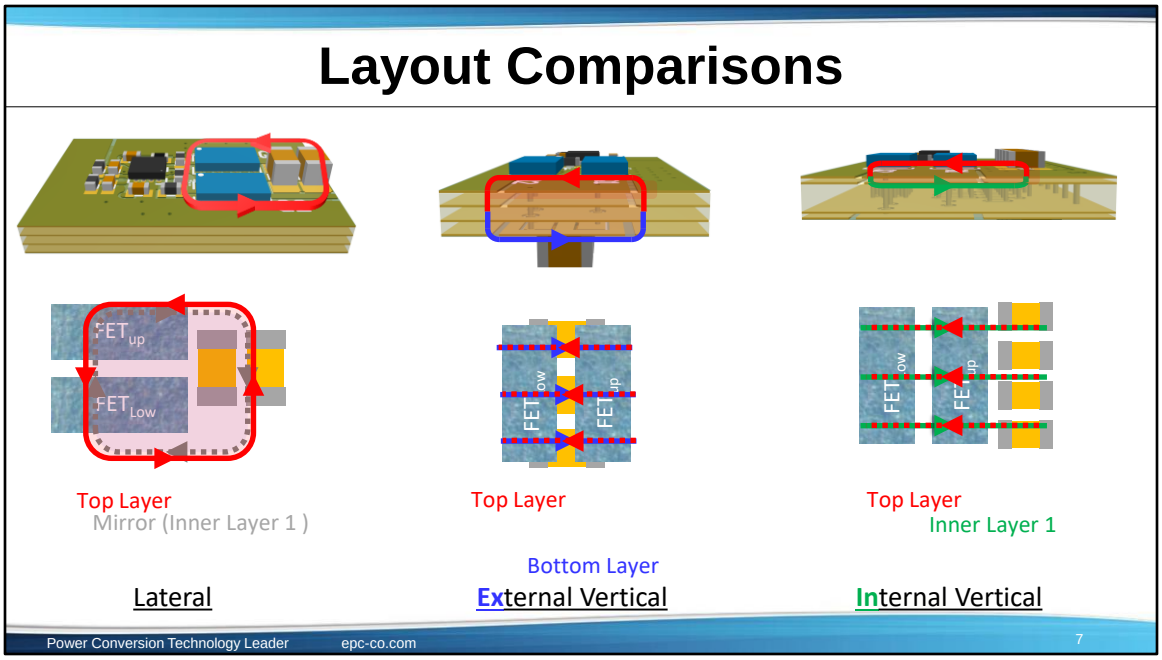


Turn Off



Turn On

Finally we will look into the effect of the gate loop inductance on losses generated in the converter. In this case there are 2 loops to consider which are the [1] turn-on and [2] turn-off. In both cases an additional resistance is used to damp out the effect of the inductance to ensure ringing voltages peaks to not exceed the maximum in the case of turn-on, ringing above the threshold voltage for turn-off. As gate loop inductance increases so does the resistance needed to damp the ringing. As the gate resistances increase so do the transition times with corresponding increase in losses. The best method to over-come gate-loop inductance is to minimize it. We'll show you how layout can achieve this and follows essentially the same methodology as that used in the power loop.

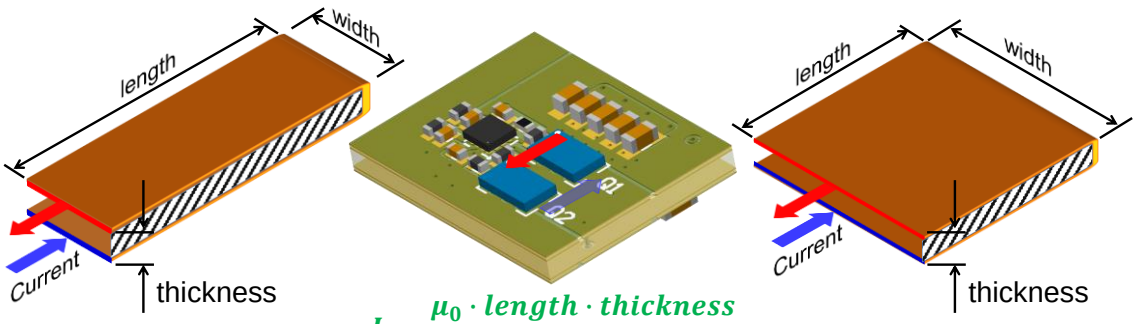


Now that we know which parasitic inductances are at play in a layout we can then begin to analyze various layout configurations. First we'll present the lateral layout characterized by the main bus capacitors placed next to the FETs such that the power loop is laterally oriented in plane with the PCB surface. This layout is popular among designers as it is simple and intuitive. [1] Next, we'll examine the external vertical layout which is also popular among designers who are familiar with double component sided designs. This layout is characterized by the vertical orientation of the power loop where the bus capacitors are placed on the bottom side of the board and the FETs on the top side of the board. [2] Finally we have the internal vertical layout, also known as the optimal layout. This layout has the bus capacitors placed next to the FETs, and the power loop is now formed vertically and uses this first inner layer for the power loop return.

Ref: D. Reusch, J. Strydom, "Understanding the Effect of PCB Layout on Circuit Performance in a High Frequency Gallium Nitride Based Point of Load Converter," APEC 2013, IEEE Transactions on Power Electronics 2014

How Inductance Manifests in a Layout

Which layout has higher inductance?



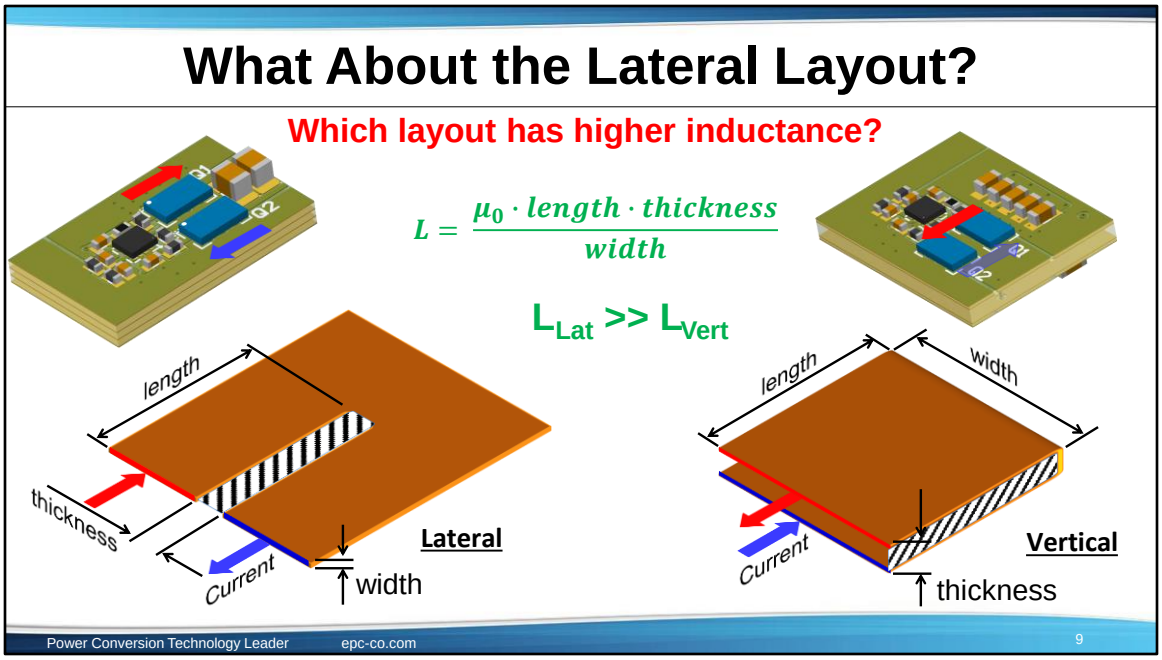
$$L = \frac{\mu_0 \cdot length \cdot thickness}{width}$$

Long, Narrow

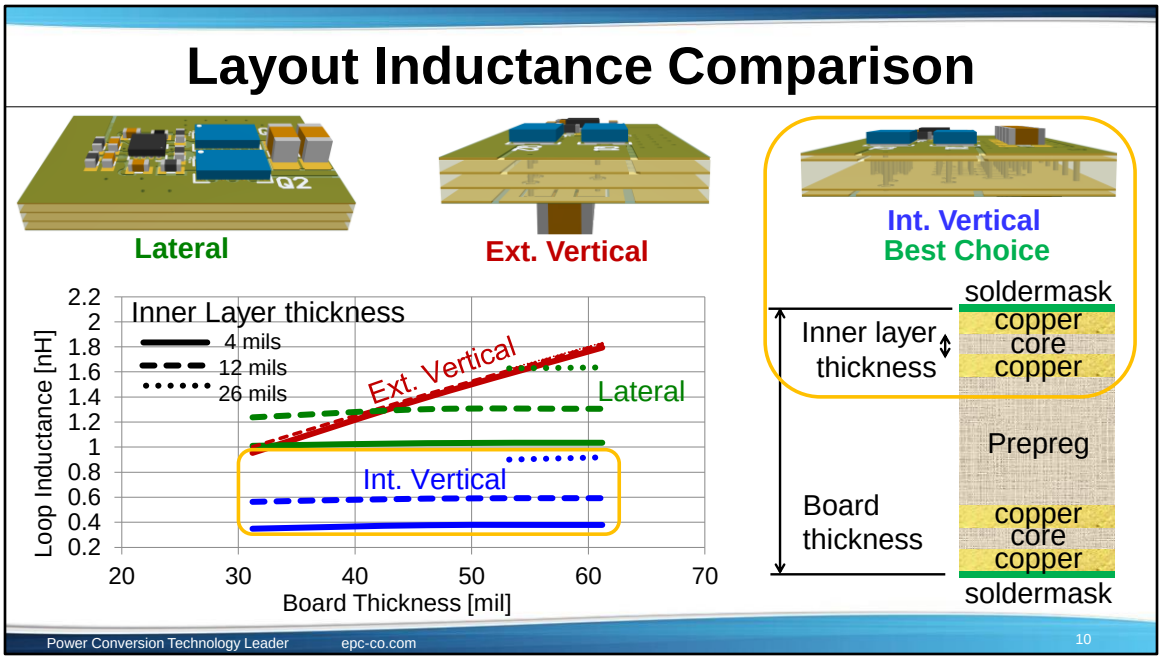
Short, Wide

$L_{LN} > L_{SW}$

To better understand which layouts will yield lower inductance we need to understand how inductance is generated. Here we show a vertical layout with the bus capacitors placed next to the FETs. In this example we ask you to identify which layout has higher inductance, the left design with its long narrow approach or the right design with its short wide approach? In both cases the thickness will be kept the same **pause** To answer this question we need to look at the magnetic flux direction and [1] using a basic air core inductor equation. From this we can see that length appears above the line and width below the line in the equation and hence if you answered the long narrow approach is higher, [2] then you are correct.



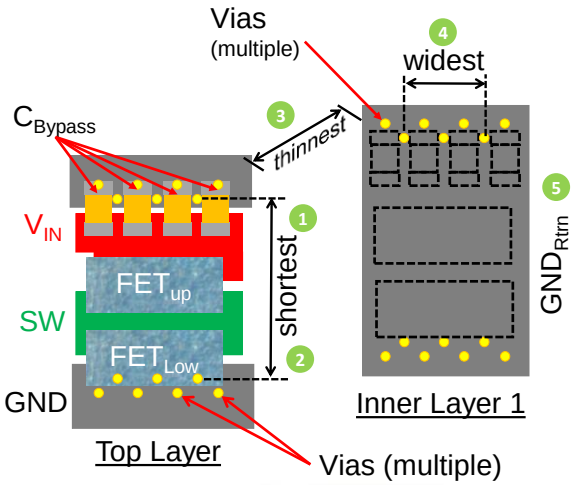
Let's shake up the design a little and compare vertical and lateral designs. We again ask the question which design has higher inductance. ***pause*** For the lateral design the definitions have changed so we need to adjust what we define as length and width. [1] Plugging those definitions into our equation we can now see that width has become a very small value below the line in the equation thus driving a significant increase in inductance. So if you answered that the lateral design has higher inductance then you are correct [2]. However, this is an incomplete picture since most lateral designs will include layers beneath the main power loop so we will examine the effect that planes have on the inductance.



With our improved understanding of inductance, we can now revisit our 3 layout designs and compare them. The lateral design is showing true to the equation as having high inductance but not as high as predicted. This is due to the first inner layer acting as a current mirror and cancelling the inductance. It is clear that as the first inner layer moves further from the power loop, its effect is an ever-increasing inductance given the current mirror effect diminishes with distance. The external vertical layout is highly dependent on the thickness of the board where as the board thickness increases, so does the power loops inductance. Finally the internal vertical layout approach has the lowest inductance given the main inductance cancellation effect occurs within the first inner layer, thus making it the [1] clear choice for the lower inductance layout.

Getting to a Low Inductance Layout

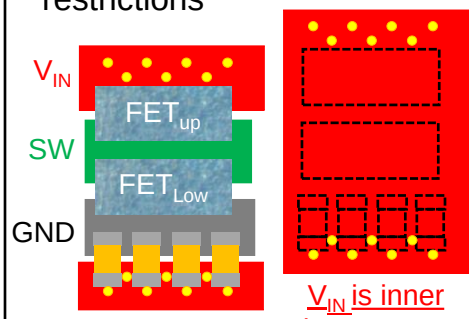
1. Vertically place components as close as possible
2. Place vias as close to the innermost electrical connection
3. Thinnest permissible substrate thickness between outer and first inner layer
4. Spread out via connections at innermost connect
5. GND return does **not** need to carry full current



Lets get into the details of how to design an internal vertical layout. [1] First we place the components as close as possible to each other without violating manufacturability rules. In this example we identify the grey trace as ground, red as the main voltage source and green as the switch-node. We show here the top and inner layer 1 layouts with the placement of the FETs and bus capacitors. [2] Next, we place the vias as close as possible to yield the shortest connection path between the two ground connections. [3] We then specify the thinnest possible substrate between the top layer and inner layer 1. [4] Now we need to create a wide as possible path for the current by spreading out the vias as much as possible. This will give us the lowest inductance solution. It should be noted that designs will have other layers that can be used for additional current paths and [5] that inner layer 1 is not required to carry the full current in the loop.

Alternative Layout Configurations

- Improves cooling for upper FET
- Useful for specific layout restrictions

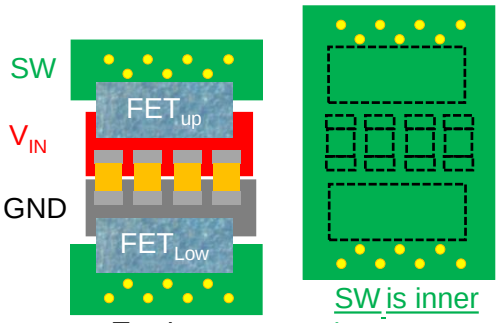


Top Layer

V_{IN} is inner layer return

Bus capacitors beside lower FET

- Buries SW-node inside the board
  - Reduces E-field EMI



Top Layer

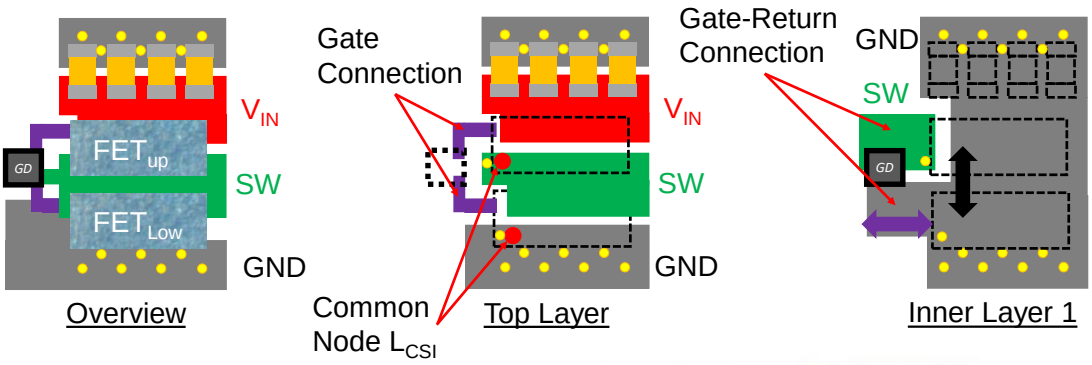
SW is inner layer return

Bus capacitors between the FETs

Now that we understand how to design an internal vertical layout, we can also look at alternative configurations. These can be useful when faced with layout restrictions or improve the thermal performance of our design as we'll show later in this presentation. On the left we show a layout where the bus capacitors are located next to the lower FET instead of the upper FET. In this case the return on the inner layer becomes the main supply Vin. This can be used when faced with layout restrictions such as a 2-phase design. It can also improve cooling for the FET given the change in via structure as we'll show in the thermal webinar of this summer series. [1] On the right we show a layout where the bus capacitors are located between the FETs and the return becomes the switch-node. In this case the switch-node becomes buried between electrically quiet planes and can thus reduce EMI.

What About the Gate Connection

- Treat the gate loop inductance same as power loop
- Orthogonal gate to power connection reduces coupling between them



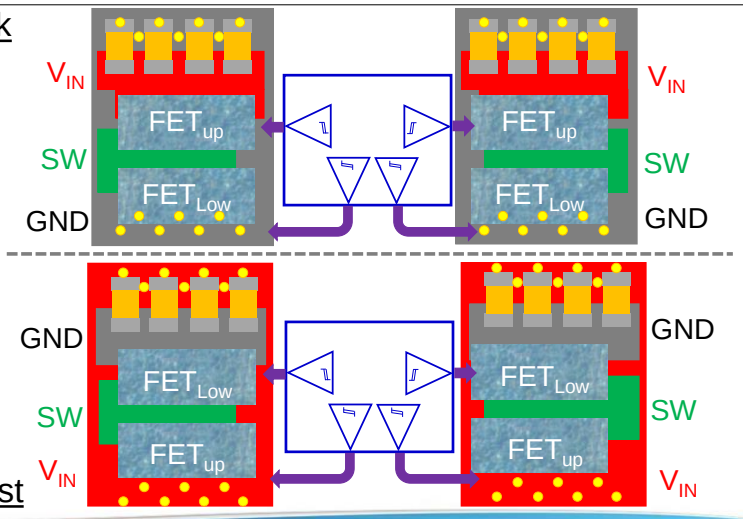
Up to now we have only discussed the power connections. Next, we need to look at how to work with the gate signals and minimize common-source inductance simultaneously. In principle we treat the gate circuits in the same manner as the power loop. Shown here, we have the gate signal on the top layer and the gate return on the inner layer. In this manner we can also locate the common coupling point close to the gate driver and thus ensure lowest possible common-source inductance. [1] To further ensure low common-source inductance, we also route the gate signal orthogonally to that of the power loop.

Single IC Dual Driver - Option 1

Buck

Prioritize the **switch**

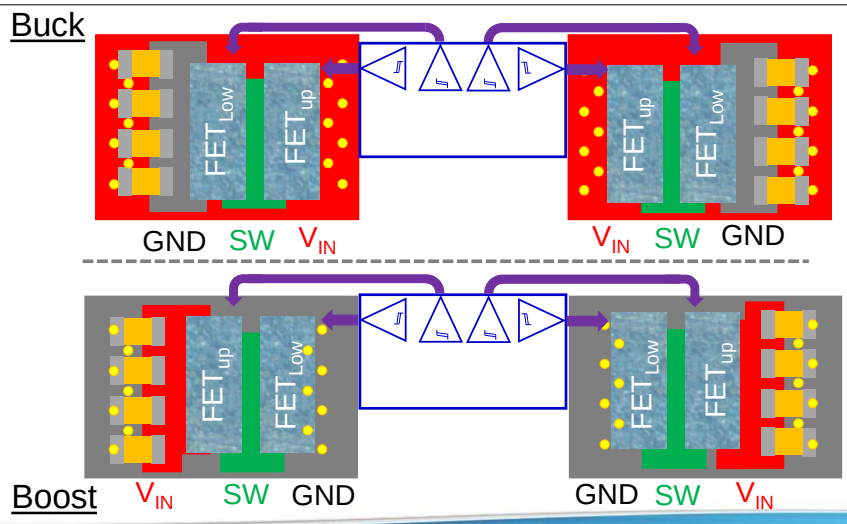
- Lowest inductance path
- Buck = upper FET
- Boost = lower FET



Boost

Now that we can route a basic half-bridge, we need to look at options with dual gate drivers in a single IC. In these situations, it may be necessary to extend the gate signal length to reach the FETs so that must be considered. The layout should always prioritize the switch and give it the lowest gate loop inductance. Since the opposite device acts as a rectifier, the gate signal is less critical and thus can be placed further away and the added inductance damped out using a higher gate resistor value as discussed earlier. Here we show configurations for a buck or a [1] boost converter for a layout design option 1 with a horizontal based layout for the FETs suitable for converters with dual output voltages.

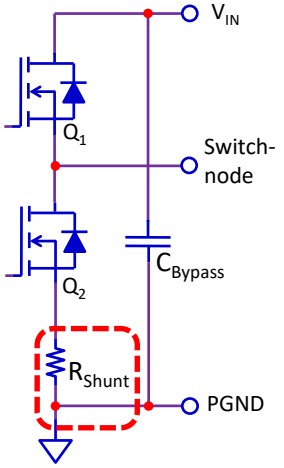
Single IC Dual Driver - Option 2



Next, we show an alternative layout configuration option for a buck or a [1] boost converter for a layout design option 2 with a vertical based layout for the FETs suitable for 2-phase single output converters.

Considerations for a Source Shunt

- Treat shunt the same as the decoupling capacitors
- Shunt must be lowest possible inductance

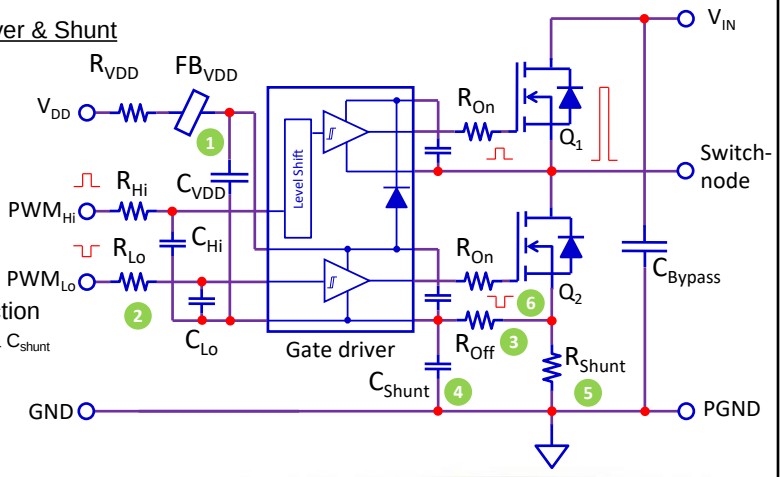


Up to now we have discussed a standard half-bridge topology. However, there may be situations where a design requires a shunt in the source path of the lower FET. [1] Essentially, we treat the shunt in the same manner as the high frequency bus capacitors, so we need to use shunts with the lowest possible inductance. We can do this in a number of ways. First our preferred approach is [2] to use multiple resistors in parallel to yield a low inductance shunt as we have learned that short wide layouts yield the lowest inductance. Alternatively, we can choose wide and narrow standard shunt. Long narrow shunts should be avoided as those have high inductance.

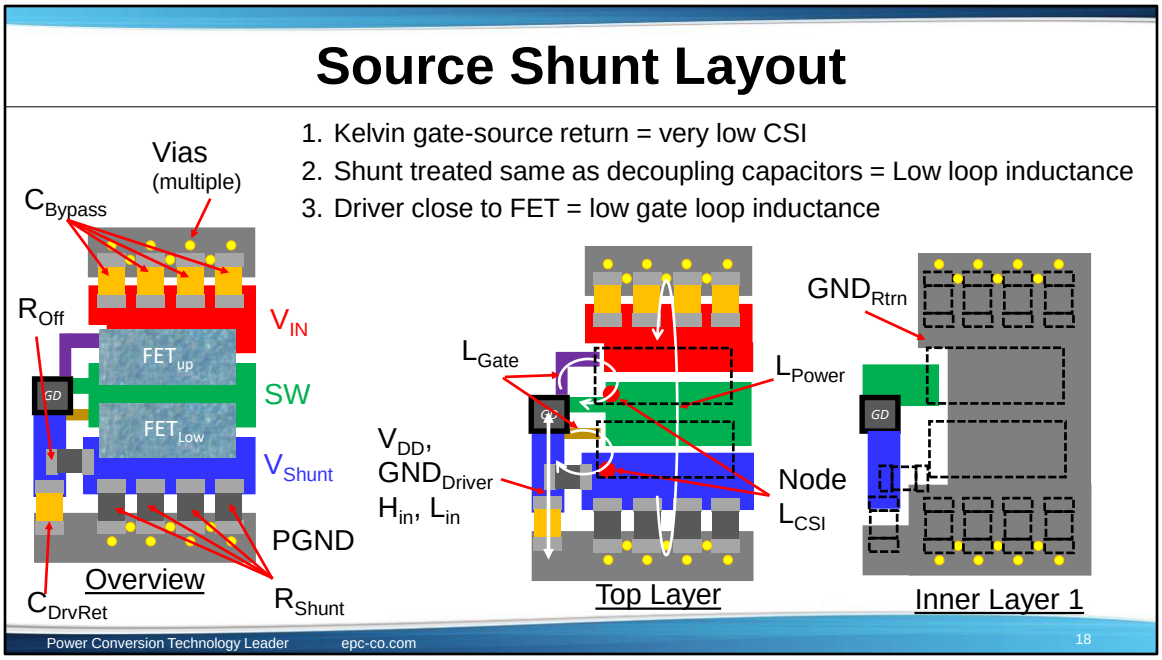
Implementing a Source Shunt

Half-Bridge with Non-Isolated Driver & Shunt

1. Filter the Gate driver supply
2. Filter the PWM signals
3. Move R_{Off} to return path
4. Filter the Shunt path
5. Limit Shunt voltage
   - Driver input hysteresis
   - Driver levels
6. Shunt Driver common connection
   - Signal return must follow ground via C_{shunt}



Adding a shunt to your schematic requires some additional considerations given the fast transitions of GaN FETs. [1] First, we need to filter the power supply to the gate driver as it is no longer connected directly to ground at high frequency. [2] The PWM signals to the driver also need filtering and just enough to maintain signal integrity. Like MOSFETs, GaN FET can have different turn-on and turn-off gate resistor values. [3] We can take advantage of this by moving the turn-off resistor to the return path thus providing additional impedance for the gate driver return and ground. [4] If additional filtering is needed, then a capacitor can now be added without affecting the shunt impedance. [5] The choice of gate driver must also look at drive levels and drive signal hysteresis and ensure those values do not fall within the shunt voltage. [6] Lastly, we still need to keep an eye on the common-source connection point as multiple paths can exist and must be taken care in the layout.



Now that we have the schematic circuits needed to add a shunt in the source path, we can now plan the layout using all the internal vertical layout technique. We'll start with the capacitors beside the upper FET where the ground is the high frequency return on the inner layer configuration. [1] Since common-source inductance is the most important we want to ensure its location will yield the lowest possible inductance. [2] We now add the shunts next to the lower FET in a similar manner as the bus capacitors. [3] We can then route the gate signals to the driver positioned as close as possible to the FETs. Lastly, the turn-off resistor and filter capacitor (if needed) and be place next to the shunt and between the FET and driver to yield the lowest inductance.

Layout Summary

- Discussed the 3 important layout-related parasitic inductances
  - Common-Source
  - Power-Loop
  - Gate-Loop
- Presented the best layout design
  - Internal-Vertical
- Provided Alternative implementations for layout
  - Input Voltage return
  - Switch-node Return

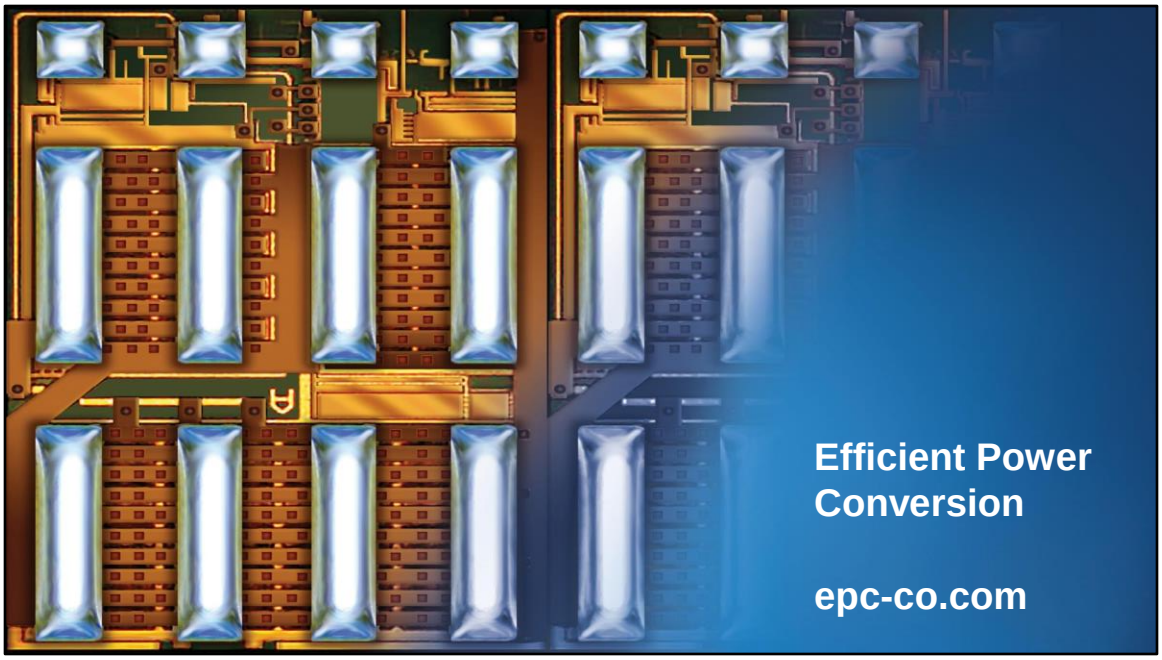
To close the layout discussion, we have learned the 3 most important layout related parasitics which are in order of importance; common-source, power loop and gate loop. [1] With that knowledge we presented various layout configurations and showed that the internal vertical yielded the lowest inductance and hence the highest converter performance. [2] Using the layout technique, we then presented alternative configurations of the internal vertical layout technique with the supply or switch-node as the return path.

Additional Resources

- App Note: How to Design an eGaN® FET-Based Power Stage with an Optimal Layout
- App Note: Designing PCB Footprint for EPC eGaN® FETs and ICs
- App Note: How to Manually Assemble an eGaN® FET or IC
- App Note: Assembling eGaN® FETs and Integrated Circuits
- Video: Footprint Design – PCB CAD System Independent
- Video: Manual Assembly – eGaN FET Die Attachment Tutorial
- Reliability: Reliability Report - Phase 12

Next Webinars

- July 28, 2021
  Gate Drivers for GaN FETs
- August 11, 2021
  Understanding the Impact of Dead-time, Q_{RR}, and C_{OSS}
- August 25, 2021
  Thermal Management of GaN FETs



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